WHAT IS CLAIMED IS:

1. A memory device having a destructive read process, comprising:

at least one block of memory cells;

a metadata block associated with each of the blocks of memory cell;

a counter within each metadata block, wherein the counter is operable to track usage of the block of memory cells associated with the metadata block.

2. The memory device of claim 1, wherein the memory device further comprises a polymer ferroelectric memory device.

3. The memory device of claim 1, wherein the memory device is used as a disk replacement.

4. The memory device of claim 1, wherein the memory device is used as a non-volatile cache memory.

5. The memory device of claim 1, wherein the metadata block further comprises flags set and reset during cache operations.

6. A method of tracking usage of a destructive read memory device, the method comprising:

participating an a memory access cycle;

incrementing a counter producing an incremented counter, wherein the counter is contained in metadata for a block participating in the memory access cycle;

updating a preexisting error correction code producing an updated error correction code, wherein the error correction code includes new data from the memory access cycle and the incremented counter; and

determining if the counter exceeds a predetermined threshold.

7. The method of claim 6, wherein the memory access cycle further comprises:

reading a sector of memory; and

correcting data from the sector of memory as necessary using the preexisting error correction code producing corrected data.

8. The method of claim 7, wherein the method further comprises writing the corrected data, the incremented counter and the updated error correction code to the memory block.

9. The method of claim 6, wherein the memory access cycle further comprises erasing a sector and reading the counter.

10. The method of claim 9, wherein the method further comprises writing new data, the incremented counter, and the updated error correction code to the memory sector previously erased.

11. The method of claim 6, wherein incrementing a wear out counter further comprises:

generating a random number;

comparing the random number to a scaling threshold;

incrementing the wear out counter, if the random number is less than the scaling threshold;

writing the wear out counter to a metadata block of a memory.

12. The method of claim 6, wherein incrementing a wear out counter further comprises:

incrementing a second counter for each memory access cycle;

determining if the second counter has reached a value substantially equal to a number of bits for the wear out counter divided by a usage threshold; and

incrementing the wear out counter if the second counter has reached the value.

13. A method of updating a counter, the method comprising:

generating a random number;

comparing the random number to a scaling threshold;

incrementing the counter, if the random number has a predetermined relationship to the scaling threshold;

writing the incremented counter to a metadata block of a memory.

14. The method of claim 13, wherein the number of bits for a counter is four.

15. The method of claim 13, wherein the predetermined relationship further comprises the random number being less than the scaling threshold.

16. A method comprising:

comparing a random number to a first predetermined threshold according to a criterion; and

if the random number meets the criterion, incrementing a counter.

17. The method of claim 16 further comprising storing the incremented counter.

18. The method of claim 16, wherein the counter is used in a destructive read memory.

19. The method of claim 16, wherein the counter is used in a polymer ferroelectric memory.

20. A memory device, comprising:

at least one block of memory cells;

a metadata block associated with each of the blocks of memory cell;

a counter located on the memory device associated with each metadata block, wherein the counter is operable to track usage of the block of memory cells associated with the metadata block.

21. The memory device of claim 20, wherein the memory device further comprises a polymer memory device.

22. The memory of claim 20, wherein the memory device further comprises a ferroelectric memory device.

23. The memory device of claim 20, wherein the memory device is used as a disk replacement.

24. The memory device of claim 20, wherein the memory device is used as a non-volatile cache memory.

25. The memory device of claim 20, wherein the metadata block further comprises flags set and reset during cache operations.

26. A method of tracking usage of a memory device, the method comprising:

participating an a memory access cycle;

incrementing a counter producing an incremented counter, wherein the counter is associated with a metadata block for a block participating in the memory access cycle;

updating a preexisting error correction code producing an updated error correction code, wherein the error correction code includes new data from the memory access cycle and the incremented counter; and

determining if the counter exceeds a predetermined threshold.

27. The method of claim 26, wherein incrementing a counter further comprises incrementing a hardware counter implemented in logic on the memory device.

28. The method of claim 26, the method comprising tracking usage of a polymer memory device.